CLAIMS

What is claimed is:

1. A high-speed receiver comprising:

a receiver termination network that includes:

a DC matched termination circuit operably coupled to provide a termination of a transmission line coupling the high-speed receiver to a transmission source and to receive high-speed data via the transmission line; and

an AC coupled bias circuit operably coupled to provide a common mode reference and to high pass filter the high-speed data to produce the filtered high-speed data;

a receiver analog front-end biased in accordance with the common mode reference, wherein the receiver analog front-end is operably coupled to amplify the filtered high-speed data to produce amplified high-speed data; and

a data recovery module operably coupled to recover data from the amplified high-speed data.

2. The high-speed receiver of claim 1, wherein the DC matched termination circuit comprises:

first resistor having an impedance corresponding to impedance of the transmission line; and

second resistor having an impedance corresponding to the impedance of the transmission line, wherein the first and second resistors are coupled in series and the series combination of the first and second resistors is coupled to the transmission line.

3. The high-speed receiver of claim 2, wherein the DC matched termination circuit further comprises:

a termination biasing integrated circuit pad operably coupled to a center node of the series combination of the first and second resistors to provide selective coupling of the center node to a supply voltage, to a supply return voltage, or to a mid-supply voltage for proper termination of the transmission source.

4. The high-speed receiver of claim 2, wherein the AC coupled bias circuit comprises:

first capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the first resistor;

second capacitor having a first plate and a second plate, wherein the first plate of the second capacitor is operably coupled to the second resistor;

first impedance having a first node operably coupled to the second plate of the first capacitor; and

second impedance having a first node operably coupled to the second plate of the second capacitor, wherein a second node of the first impedance is operably coupled to a second node of the second impedance and coupled to a bias voltage, wherein impedance of the first and second impedances is at least one order of magnitude greater than the impedance of the first and second resistors, and wherein capacitance of the first and second capacitors, in combination with the first and second impedances, establish a corner frequency for the high-pass filter.

5. The high-speed receiver of claim 4, wherein each of the first and second capacitors further comprises:

the first plate and second plate configured in a finger arrangement to produce a capacitor structure; and

a doping block encompassing the capacitor structure to provide an impedance in series with parasitic capacitance of the capacitor structure.

6. The high-speed receiver of claim 4, wherein each of the first and second capacitors further comprises:

the first plate being fabricated on at least two metal layers operably coupled with a first via; and

the second plate being fabricated on the at least two metal layers operably coupled with a second via.

7. The high-speed receiver of claim 1, wherein the DC matched termination circuit comprises:

a resistor having an impedance corresponding to impedance of the transmission line.

8. The high-speed receiver of claim 7, wherein the AC coupled bias circuit comprises:

a capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the resistor; and

a bias impedance having a first node operably coupled to the second plate of the first capacitor and a second node coupled to a supply return, wherein impedance of the bias impedance is at least one order of magnitude greater than the impedance of the resistor, and wherein capacitance of the capacitor, in combination with the bias impedance, establish a corner frequency for the high-pass filter.

9. A multi-gigabit transceiver comprising:

transmit section operably coupled to convert parallel output data into high-speed output serial data; and

receiver section that includes:

a receiver termination network that includes:

a DC matched termination circuit operably coupled to provide a termination of a transmission line coupling the high-speed receiver to a transmission source and to receive high-speed serial data via the transmission line; and

an AC coupled bias circuit operably coupled to provide a common mode reference and to high pass filter the high-speed serial data to produce the filtered high-speed serial data;

a receiver analog front-end biased in accordance with the common mode reference, wherein the receiver analog front-end is operably coupled to amplify the filtered high-speed serial data to produce amplified high-speed serial data; and

a data recovery module operably coupled to recover data from the amplified high-speed serial data.

10. The multi-gigabit transceiver of claim 9, wherein the DC matched termination circuit comprises:

first resistor having an impedance corresponding to impedance of the transmission line; and

second resistor having an impedance corresponding to the impedance of the transmission line, wherein the first and second resistors are coupled in series and the series combination of the first and second resistors is coupled to the transmission line.

11. The multi-gigabit transceiver of claim 10, wherein the DC matched termination circuit further comprises:

a termination biasing integrated circuit pad operably coupled to a center node of the series combination of the first and second resistors to provide selective coupling of the center node to a supply voltage, to a supply return voltage, or to a mid-supply voltage for proper termination of the transmission source.

12. The multi-gigabit transceiver of claim 10, wherein the AC coupled bias circuit comprises:

first capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the first resistor;

second capacitor having a first plate and a second plate, wherein the first plate of the second capacitor is operably coupled to the second resistor;

first impedance having a first node operably coupled to the second plate of the first capacitor; and

second impedance having a first node operably coupled to the second plate of the second capacitor, wherein a second node of the first impedance is operably coupled to a second node of the second impedance and coupled to a bias voltage, wherein impedance of the first and second impedances is at least one order of magnitude greater than the impedance of the first and second resistors, and wherein capacitance of the first and second capacitors, in combination with the first and second impedances, establish a corner frequency for the high-pass filter.

13. The multi-gigabit transceiver of claim 9, wherein the DC matched termination circuit comprises:

a resistor having an impedance corresponding to impedance of the transmission line.

14. The multi-gigabit transceiver of claim 13, wherein the AC coupled bias circuit comprises:

a capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the resistor; and

bias impedance having a first node operably coupled to the second plate of the first capacitor and a second node coupled to a supply return, wherein impedance of the bias impedance is at least one order of magnitude greater than the impedance of the resistor, and wherein capacitance of the capacitor, in combination with the bias impedance, establish a corner frequency for the high-pass filter.

15. An integrated circuit capacitor comprising:

a first plate fabricated on a metal layer having a first geometric shape;

a second plate fabricated on the metal layer having a second geometric shape, wherein the first and second geometric shapes form a finger arrangement to produce a capacitor structure; and

doping block encompassing the capacitor structure to provide an impedance in series with parasitic capacitance of the capacitor structure.

16. The integrated circuit capacitor of claim 15 further comprising:

the first plate further being fabricated on a second metal layer having the first geometric shape, wherein the first geometric shape of the second metal layer is coupled to the first geometric shape on the metal layer by a via; and

the second plate further being fabricated on the second metal layer having the second geometric shape, wherein the second geometric shape of the second metal layer is coupled to the second geometric shape on the metal layer by a second via.

17. A receiver termination network comprising:

a DC matched termination circuit operably coupled to provide a termination of a transmission line coupling a high-speed receiver to a transmission source and to receive high-speed data via the transmission line; and

an AC coupled bias circuit operably coupled to high pass filter the high-speed data to produce filtered high-speed data and operably coupled to produce a common mode reference.

18. The receiver termination network of claim 17, wherein the DC matched termination circuit comprises:

first resistor having an impedance corresponding to impedance of the transmission line; and

second resistor having an impedance corresponding to the impedance of the transmission line, wherein the first and second resistors are coupled in series and the series combination of the first and second resistors is coupled to the transmission line.

19. The receiver termination network of claim 18, wherein the DC matched termination circuit further comprises:

a termination biasing integrated circuit pad operably coupled to a center node of the series combination of the first and second resistors to provide selective coupling of the center node to a supply voltage, to a supply return voltage, or to a mid-supply voltage for proper termination of the transmission source.

20. The receiver termination network of claim 18, wherein the AC coupled bias circuit comprises:

first capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the first resistor;

second capacitor having a first plate and a second plate, wherein the first plate of the second capacitor is operably coupled to the second resistor;

first impedance having a first node operably coupled to the second plate of the first capacitor; and

second impedance having a first node operably coupled to the second plate of the second capacitor, wherein a second node of the first impedance is operably coupled to a second node of the second impedance and coupled to a bias voltage, wherein impedance of the first and second impedances is at least one order of magnitude greater than the impedance of the first and second resistors, and wherein capacitance of the first and second capacitors, in combination with the first and second impedances, establish a corner frequency for the high-pass filter.

21. The receiver termination network of claim 20, wherein each of the first and second capacitors further comprises:

the first plate and second plate configured in a finger arrangement to produce a capacitor structure; and

a doping block encompassing the capacitor structure to provide an impedance in series with parasitic capacitance of the capacitor structure.

22. The receiver termination network of claim 20, wherein each of the first and second capacitors further comprises:

the first plate being fabricated on at least two metal layers operably coupled with a first via; and

the second plate being fabricated on the at least two metal layers operably coupled with a second via.

23. The receiver termination network of claim 18, wherein the DC matched termination circuit comprises:

a resistor having an impedance corresponding to impedance of the transmission line.

24. The receiver termination network of claim 23, wherein the AC coupled bias circuit comprises:

a capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the resistor; and

a bias impedance having a first node operably coupled to the second plate of the first capacitor and a second node coupled to a supply return, wherein impedance of the bias impedance is at least one order of magnitude greater than the impedance of the resistor, and wherein capacitance of the capacitor, in combination with the bias impedance, establish a corner frequency for the high-pass filter.